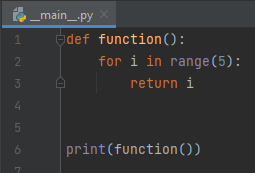
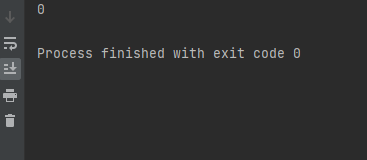
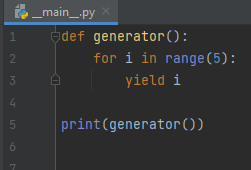
# Background information

**A small tutorial on generators**

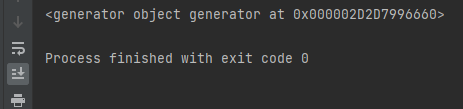
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Po uruchomieniu symulacji otrzymano:

****

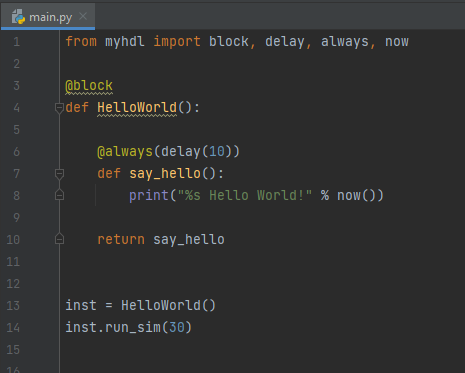
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Po uruchomieniu symulacji otrzymano:

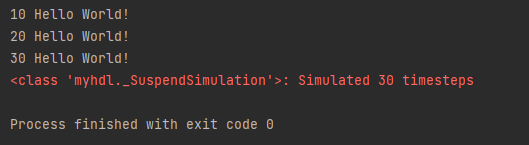
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**Introduction to MyHDL**

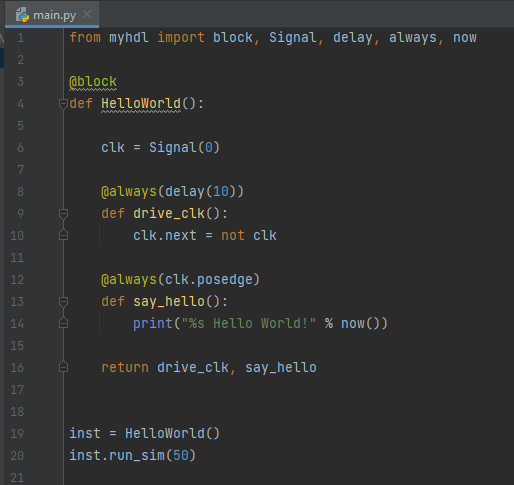
**A basic MyHDL simulation**



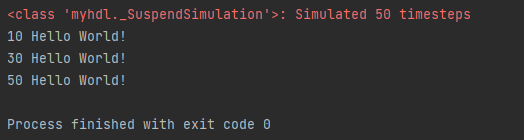
Po uruchomieniu symulacji otrzymano:



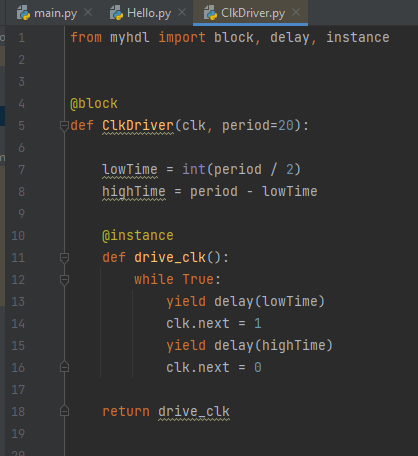
**Signals and concurrency**

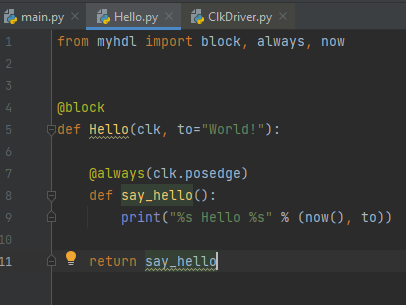


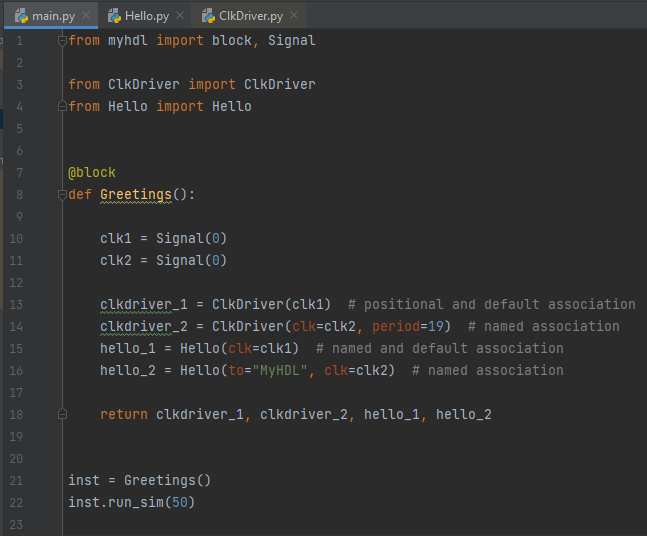
Po uruchomieniu symulacji otrzymano:



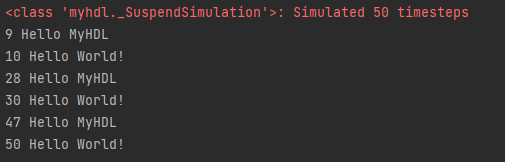
## Parameters, ports and hierarchy





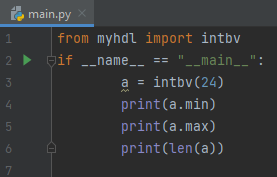


Po uruchomieniu symulacji otrzymano:

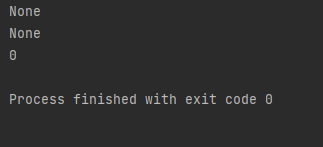


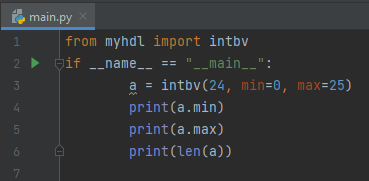
**Hardware-oriented types**

**The [intbv](http://docs.myhdl.org/en/stable/manual/reference.html" \l "myhdl.intbv" \o "myhdl.intbv) class**

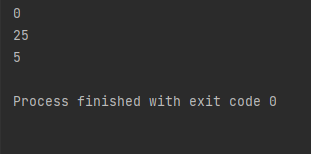
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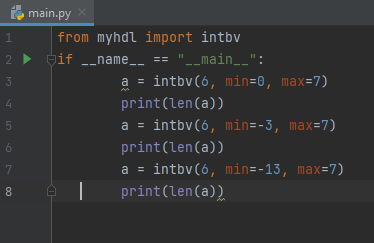
Po uruchomieniu symulacji otrzymano:

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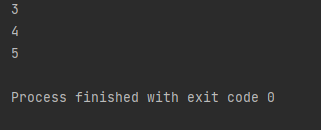
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Po uruchomieniu symulacji otrzymano:

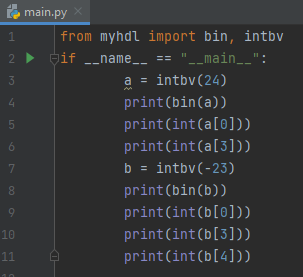
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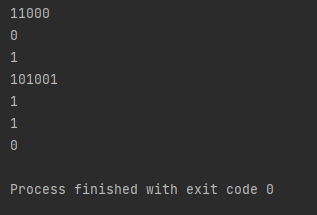
Po uruchomieniu symulacji otrzymano:

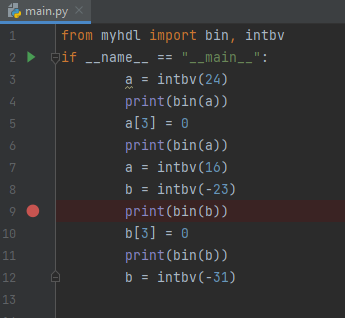


**Bit indexing**

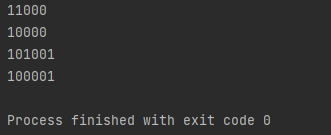


Po uruchomieniu symulacji otrzymano:

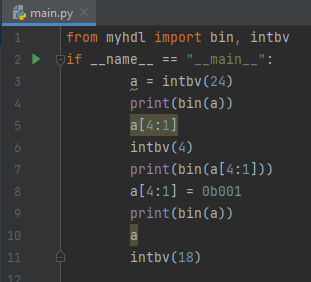




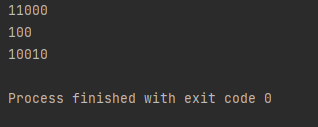
Po uruchomieniu symulacji otrzymano:

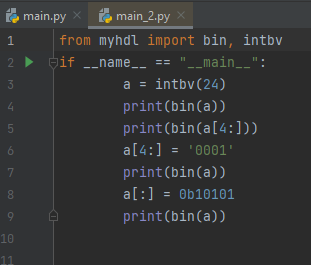


**Bit slicing**

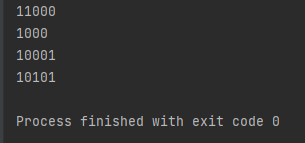


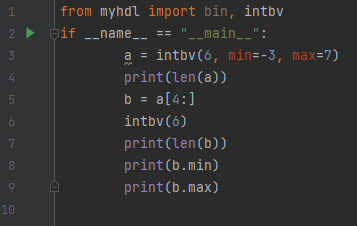
Po uruchomieniu symulacji otrzymano:



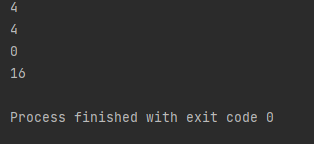


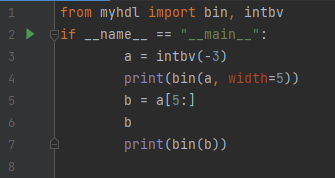
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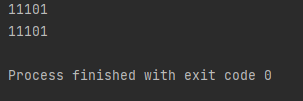


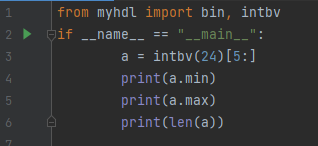
Po uruchomieniu symulacji otrzymano:



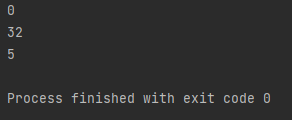


Po uruchomieniu symulacji otrzymano:

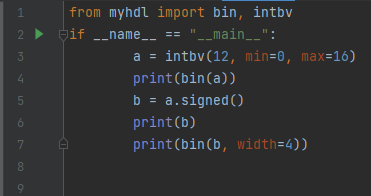




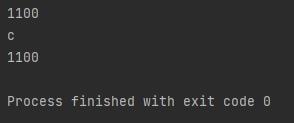
Po uruchomieniu symulacji otrzymano:



**Unsigned and signed representation**

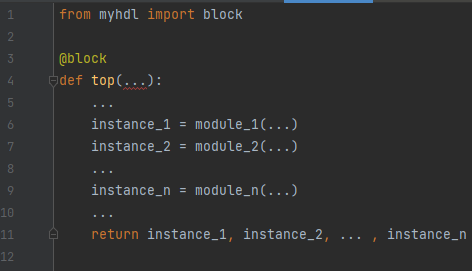


Po uruchomieniu symulacji otrzymano:

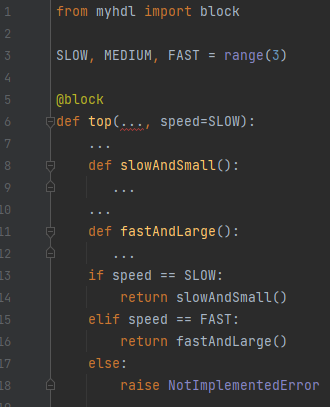


# Structural modeling

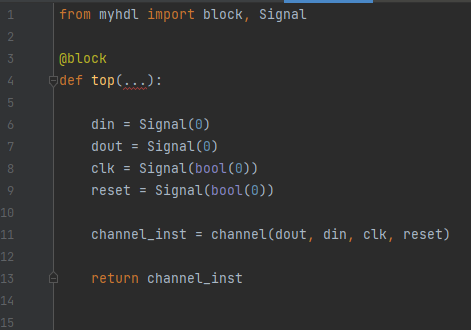
**Introduction**

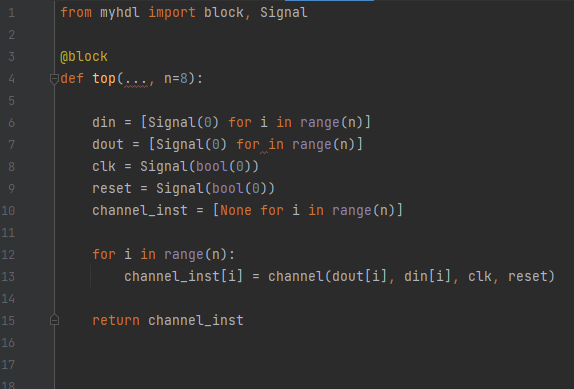


**Conditional instantiation**

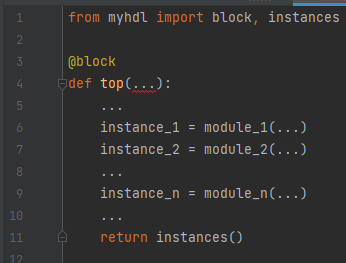


### Lists of instances and signals



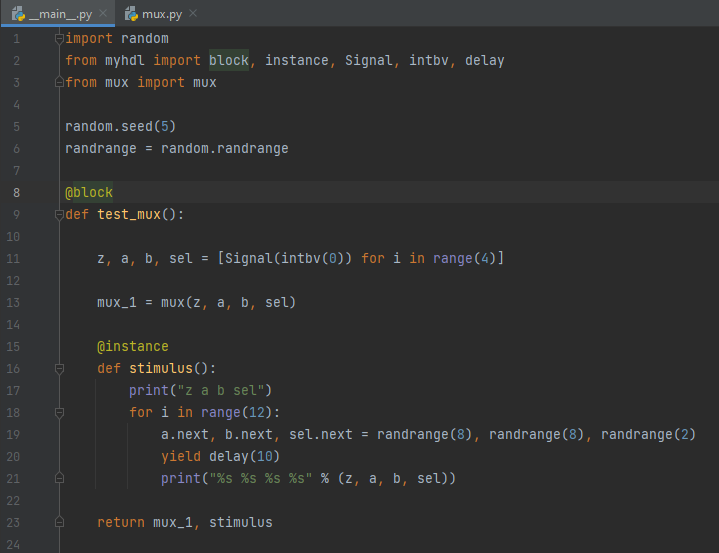


**Inferring the list of instances**



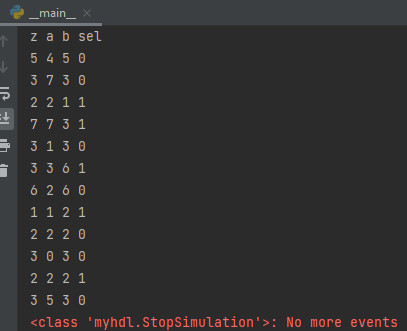
# RTL modeling

**Combinatorial logic**

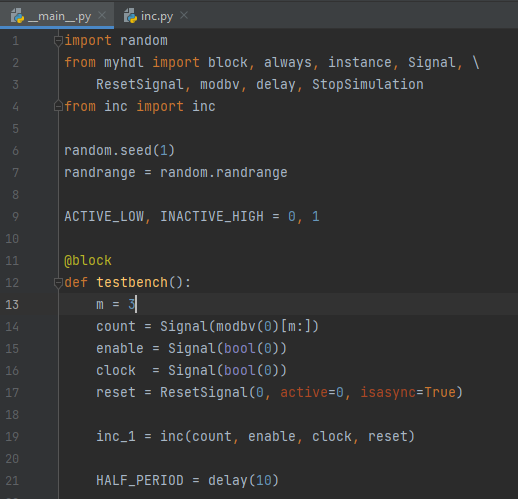


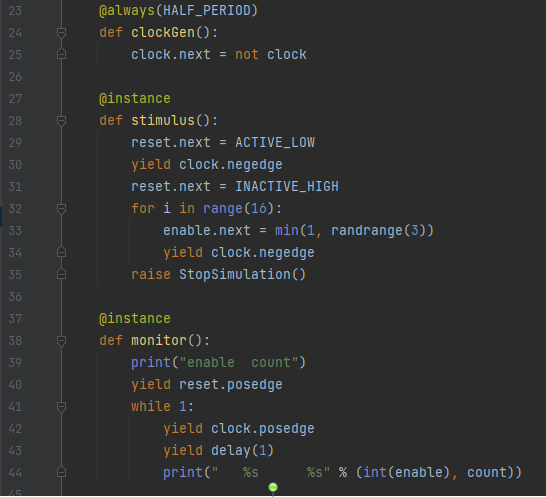


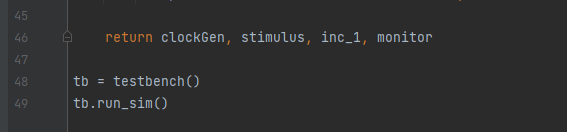
Po uruchomieniu symulacji otrzymano:



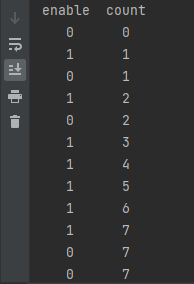
**Sequential logic**

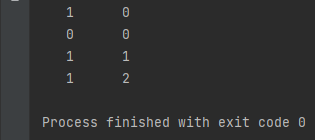




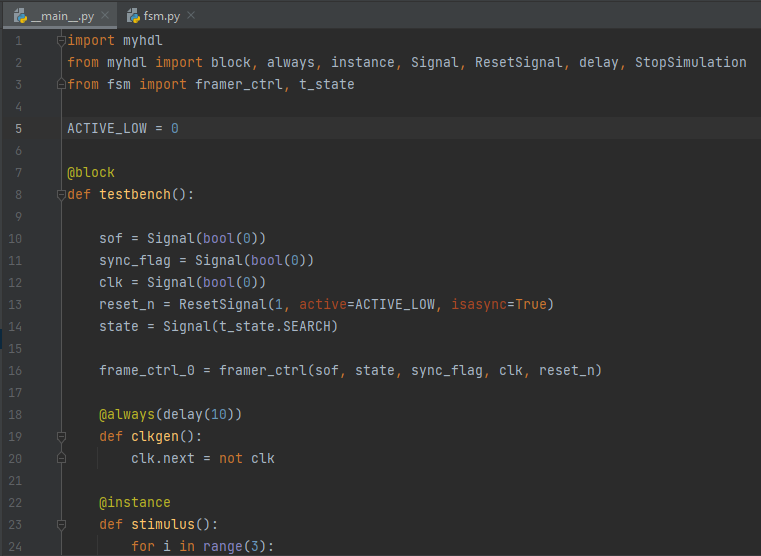


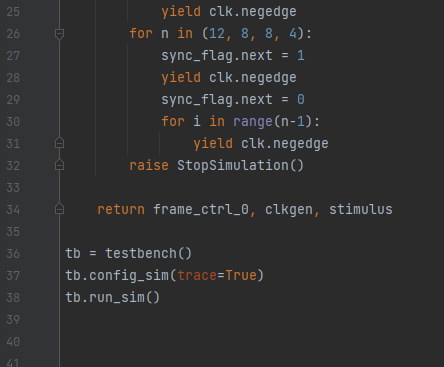
Po uruchomieniu symulacji otrzymano:

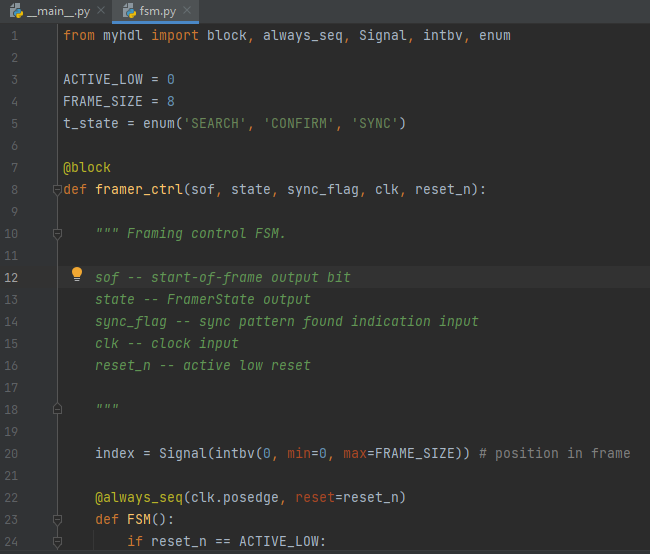


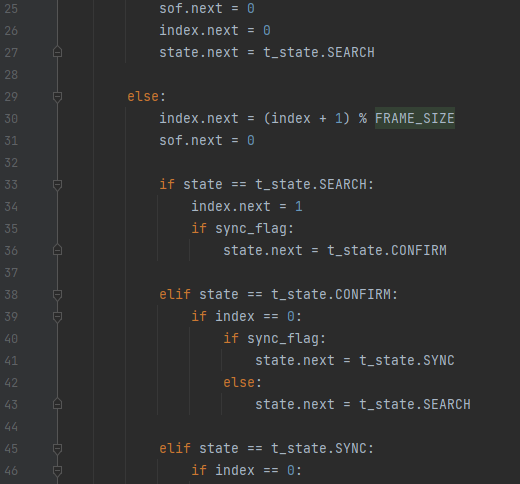


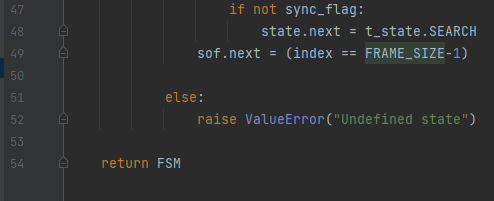
**Finite State Machine modeling**



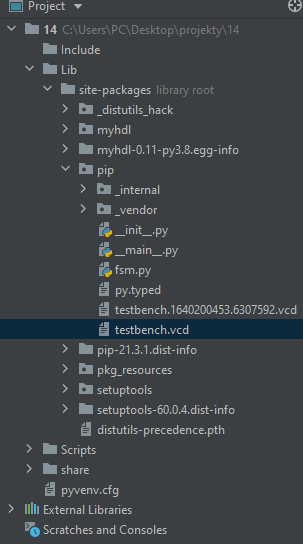






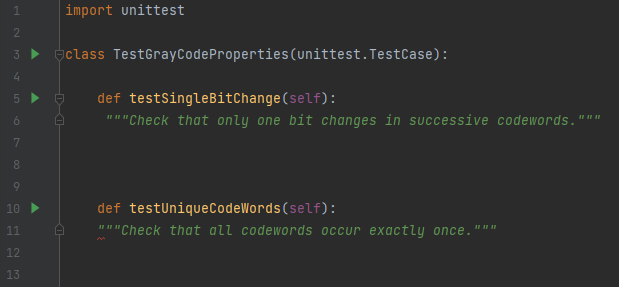


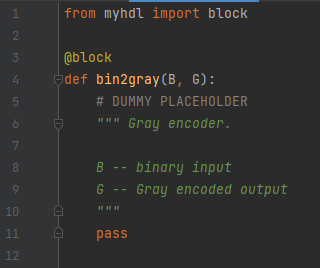
Po uruchomieniu symulacji otrzymano plik testbench.vcd dzięki któremu można zaobserwować przebiegi.

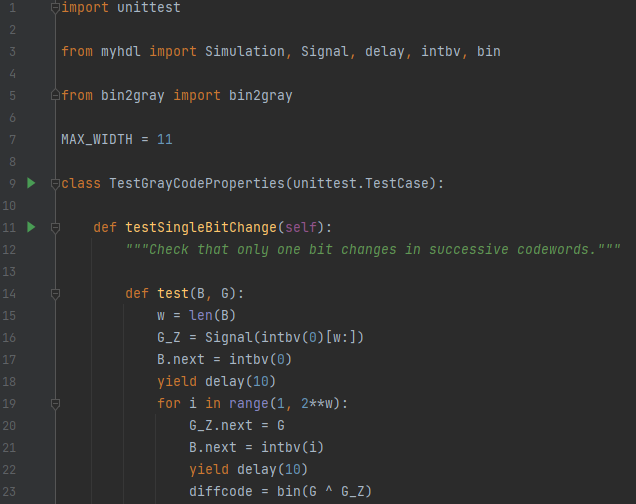


# Unit testing

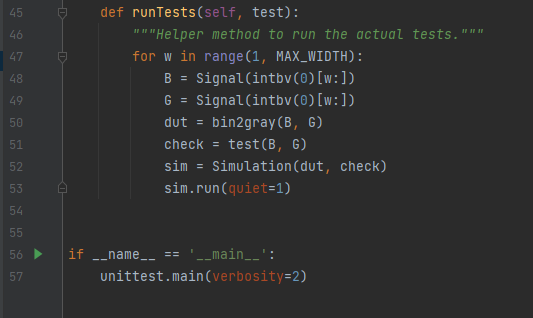
**The importance of unit tests**



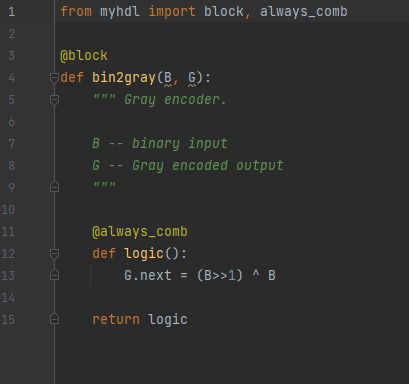




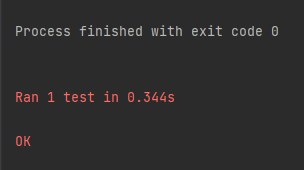




Prawidłowa implementacja „bin2gray”:



Po uruchomieniu symulacji otrzymano:



nextLn:



